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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,091	10/23/2003	Eric Hung	5201-27500	7976

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Leo Peters
LSI Logic Corporation
MS D-106
1621 Barber Lane
Milpitas, CA 95035

EXAMINER	
NGUYEN, DANG T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/692,091	HUNG ET AL.	
	Examiner	Art Unit	
	Dang T. Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14-20* is/are rejected.

7)☒ Claim(s) *13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search history*.

DETAILED ACTION

1. This action is responsive to applicant's amendment filed on 4/25/05. Claims 1 and 5 have been amended. Claims 1 – 20 are pending on this application.

2. The indicated allowability of claims 8 - 20 are withdrawn in view of the newly discovered reference(s) to Jang et al., Pub. No.: 2003/0107908 and Chu et al., U.S. Patent No.: 5,856,937. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 – 5, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Jang et al., Pub. No.: 2003/0107908.

Regarding independent claim 1, Fig. 5A, 5B, 5C and Fig. 9 of Jang et al. disclose a memory module (fig. 5 [510]), comprising: a printed circuit board (Fig. [5 [510]) having opposing first (Fig. 5 B,C [top surface of 510]) and second outside surfaces (Fig. 5 B,C [bottom surface of 510]); a via extending (Fig. 5 [531]) along an axis perpendicular to the first and second outsides surfaces and extending entirely

through the printed circuit board (Fig. 5 [510]); at least one primary semiconductor memory device (Fig. 5 B,C [150']) arranged upon the first outside surface and coupled to the primary conductor (Fig. 5 B,C [560]); a memory controller (Fig. 5A[540]) coupled to the primary conductor (Fig. 5 B,C[560]); and at least one secondary semiconductor memory device (Fig. 5B,C [150]) arranged upon the second outside surface substantially opposite the primary semiconductor memory device (Fig. 5 B,C [150') and coupled to the secondary conductor (Fig. 5 [562]).

Regarding dependent claim 2, Fig. 5 B and C of Jang et al. further discloses wherein the primary [560] and secondary [562] semiconductor memory devices [150', 150] each comprise a midpoint between outer lateral edges of each respective primary and secondary semiconductor memory device (midpoint of 560, 562) through which the single axis (531) extends substantially perpendicular to the first and second outside surfaces (top and bottom surfaces of 510).

Regarding dependent claim 3, Fig. 5 B and C of Jang et al. discloses wherein the primary [150'] and secondary [150] semiconductor memory devices each comprise outer lateral edges (110 (k, 8)) and (110 9k, 5)) that are directly opposite the printed circuit board from each other (Fig. 5 [top and bottom of 510]).

Regarding dependent claim 4, Fig. 5A of Jang et al. discloses wherein the at least one primary semiconductor memory device [150'] comprises a pair of primary semiconductor memory devices and arranged on a first portion of the first outside surface [top surface of 150], and wherein the at least one secondary semiconductor memory device [150] comprises a pair of secondary semiconductor memory devices

arranged on a second portion of the second outside surface substantially opposite the first portion (See paragraph 0005).

Regarding dependent claim 5, (See paragraph 0005) wherein a first one of the pair of primary semiconductor memory devices [150] and a first one of the pair of secondary semiconductor memory devices [paragraph 0005 discloses multiples memory chips located on both sides of the circuit board] comprise a first central point (Midpoint of 560, 562 of fig. 5B, C) through which a first axis (531) extends substantially perpendicular to the first and second outside surfaces (510) and wherein a second one of the pair of primary semiconductor memory devices and a second one of the pair of secondary semiconductor memory devices [paragraph 0005 discloses multiples memory chips located on both sides of the circuit board]comprise a second central point through which a second axis (Fig. 5B,C [564])) extends a parallel, spaced distance from the first axis substantially perpendicular to the first and second outside surfaces (510).

Regarding dependent claim 17, Fig. 5B and C of Jang et al. discloses a method for arrange memory devices (150', 150) upon a printed circuit board (510), comprising: arranging a pair of memory devices (150, 150') on opposing outside surfaces of the printed circuit board directly opposite one another with the midpoint of pair (midpoint of 560, 562) arranged upon an axis (531) that extends perpendicular to the opposing outside surfaces (top and bottom surfaces of 510); in a single steps, employing concurrent solder reflow: surface mounting at least one lead (110 (k, 8)) a first one of the pair (150') of memory devices to a first end (560) of a via (531) extending perpendicular through the printed circuit board (51) and to a first end of a

conductor (560) extending across a first one of the opposing outside surfaces (top surfaces of 510); surfaces mounting at least one lead extending from the memory controller (540) to a second oppose end of the conductor (Fig. 5A); and surface mounting at least one lead (110 (k,5)) extending from a second one (150) of the pair memory devices to a second end (562) of the via opposite the first end (562) of the via (531).

Claims 8, 14 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Chu et al., U.S. Patent No. 5,856,937 – filed: Jun 23, 1997.

Regarding independent claim 8, Figs. 2 and 6 of Chu et al. disclose a memory module, comprising: a printed circuit board (10) consisting of four conductive layers (72, 74, 76, 78) dielectrically separated from each other, wherein a first pair (72, 74) of the four conductive layers are on opposed outside surfaces of the printed circuit board (10) and a second pair (76, 78) of the four conductive layers are on dielectrically isolated, parallel inside surfaces of the printed circuit board (90, 92, 94); a plurality of primary conductors(72) arranged on one of the first pair of the four conductive layers; a plurality of secondary conductors (74) arranged on another one of the first pair of the four conductive layers; a ground supply conductor (78) arranged on one of the second pair of four conductive layers; a power supply conductor (76) arranged on another one of the second pair of four conductive layers; a primary synchronous dynamic random access memory (20) packaged integrated circuit placed in a first slot (Fig. 2 [20]) on a first one of the opposed outside surfaces (Fig. 2 [Front side]) and coupled to a subset of the plurality of primary conductors (72); a secondary synchronous dynamic random access

memory (40) packaged integrated circuit placed in a second slot (Fig. 2[20]) on a second one of the opposed outside surfaces (Fig.2[Back side]) and coupled to a subset of the plurality of secondary conductors ((74); and wherein the first (20) and second (40) slots comprise bonding pads arranged on a portion of the respective first and second ones of the opposed outside surfaces (Col. 8 lines 57 – 60) to form a footprint in which the primary SDRAM is surface mounted substantially directly opposite the secondary SDRAM (See Fig. 2, 4).

Regarding dependent claim 14, Fig. 2 of Chu et al. further comprising a memory controller (17) placed on only one of the opposed surface and coupled directly to the plurality of the primary conductors and coupled indirectly through vias extending through the printed circuit board to the plurality of secondary conductors (See Fig. 2).

Regarding dependent claim 16, Fig. 2 et al. discloses a memory module is a dual line memory module is arranged on the same printed circuit board (10) as an execution unit or processor.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6, 7 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jang et al., Pub. No.: 2003/0107908 in view of Chu et al. U.S. Patent No. 5,856,937.

Regarding claims 6 and 18, Jang et al. as applied to claims 1 and 17 above, does not explicitly disclose wherein the printed circuit board [510] further comprises: a power supply conductor arranged upon a power supply plane dielectrically spaced between the first and second outside surfaces and a ground supply conductor arranged upon a ground supply plane dielectrically spaced between the first and second outside surfaces [and also between the power supply plane and either the first outside surface or the second outside surface

Fig. 6 of Chu et al. discloses wherein the printed circuit board [10'] further comprises: a power supply conductor [76] arranged upon a power supply plane dielectrically spaced between the first and second outside surfaces (Col. 8 line 50 – Col. 9 line 23); and a ground supply conductor [78] arranged upon a ground supply plane dielectrically spaced between the first and second outside surfaces [10'] and also between the power supply plane [76] and either the first outside surface or the second outside surface (Col. 8 line 50 – Col. 9 line 23).

Jang et al. and Chu et al. are common subject matter for dual memory of printed circuit boar. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporated the power and ground plane of the PCB of Chu et al. into the PCB of Jang et al. for the purpose of providing power and

ground potential to the memory from the PCB to reduce the manufacturing cost of processor module (Chu et al., Col. 3 lines 16 – 17).

Regarding dependent claim 7, Jang et al. as applied to claim 1 above, does not explicitly disclose wherein the printed circuit board [510] further comprises wherein the printed circuit board consists of four conductive layers dielectrically separated from each other, and wherein two of the four conductive layers [74 and 72] are on the first and second outside surfaces [10'] (Col. 9 lines 11-13).

Fig. 6 of Chu et al. discloses wherein the printed circuit board consists of four conductive layers dielectrically separated from each other, and wherein two of the four conductive layers [74 and 72] are on the first and second outside surfaces [10'] (Col. 9 lines 11-13).

Jang et al. and Chu et al. are common subject matter for dual memory of printed circuit boar. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporated the PCB of Chu et al. into the PCB of Jang et al. for the purpose of providing power and ground potential to the memory from the PCB to reduce the manufacturing cost of processor module (Chu et al., Col. 3 lines 16 – 17).

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chu et al., U.S. Patent No. 5,856,937 in view of Jang et al., Pub. No.: 2003/0107908.

Fig. 6 of Chu et al. as applied to claim 8 above, does not disclose a midpoint of the bonding pad (70) is linked by an axial line to a midpoint of the bonding pad (72); wherein the axial line is perpendicular to the opposites outside surfaces.

Fig. 5B of Jang et al. discloses a midpoint of the bonding pad (560) is linked by an axial line (531) to a midpoint of the bonding pad (562)); wherein the axial line (531) is perpendicular to the opposites outside surfaces.

Chu et al. and Jang et al. are common subject matter of memory formed on both side of the circuit board. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporated the axial line taught by Jang et al. in the the axial line of Chu et al. for the purpose to simplifying the interconnection between memories formed on opposites side of the circuit board.

6. Claims 10, 11,12 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chu et al., U.S. Patent No. 5,856,937 in view of Millar U.S. Patent No. 5, 945,886.

Regarding dependent claims 10 and 11, Chu et al. as applied to claim 8 above, does not disclose the primary and secondary conductors are terminated through pull-up resistors and output drivers connected to a reference supply according to stub series terminated logic

Fig. 1 of Millar disclose a dual in line memory modules (DIMM; See Col. Of 37 – 40) having opposing first and second ends conductors (12, 13) of memory devices (11) are terminating through pull-up resistor (14) and output driver connected to a reference supply (VREF); according to stub series terminated logic (VTT).

Chuet al. and Millar are common subject matter for dual line memory modules. Therfore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporated termination of memory device taught by Millar

et al. into Jang et al. for the purpose of providing matching the loaded impedance of the conductive lines (Millar, Col. 2 lines 55 – 63).

Regarding dependent claim 12, Fig. 6 of Chu et al. combined with Jang et al. as applied to claim 10 above, further discloses the primary and secondary (20, 40) are coupled to a power supply (76).

Regarding dependent claim 15, Chu ea al. combine with Jang et al. as applied to claim 10 above, further discloses the primary and secondary memory are packaged within a thin small outline pacakage with leads extending from the solder bonded to the corresponding bonding pads of the first and second slots (Chu et al. Fig. 2).

7. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jang et al., Pub. No.: 2003/0107908, in view of Khatri et al., Pub. No.: US 2003/0137860.

Jang et al. as applied to claim 17 above, does not teach terminating the opposing first and second ends of the conductor with a pull-up resistor to a power supply having a voltage value dissimilar from a voltage value placed on the pair of packaged memory devices.

Fig. 3 of Khatri et al. discloses DIMM memory module having terminating the opposing first and second ends of the conductor with a pull-up resistor ((Fig. 4 [240]) to a power supply having a voltage value (Vtt) dissimilar from a voltage value (Vdd) placed on the pair of packaged memory devices (page 2, last five lines of paragraph 0026).

Jang et al. and Khatri et al. are common subject matter for DIMM. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention

was made to incorporate the teaching of Khatri et al. into Jang et al. for the purpose of reducing effects of reflections on the memory bus (Khatri et al., paragraph 0007).

8. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jang et al., Pub. No.: 2003/0107908, in view of Millar U.S. Patent No. 5,945,886.

Jang et al. as applied to claim 17 above, does not explicitly the opposing first and second ends conductors of memory devices are terminating with stub series terminating logic.

Fig. 1 of Millar disclose a dual in line memory modules (DIMM; See Col. Of 37 – 40) having opposing first and second ends conductors (12, 13) of memory devices (11) are terminating with stub series terminating logic (VTT).

Jang et al. and Millar are common subject matter for dual line memory modules. Therfore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporated termination of memory device taught by Millar et al. into Jang et al. for the purpose of providing matching the loaded impedance of the conductive lines (Millar, Col. 2 lines 55 – 63).

Allowable Subject Matter

9. Claim 13 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art does not teach or suggest "wherein the power supply conductor comprises at least two laterally spaced coplanar power supply conductors, and wherein one power supply conductor is coupled between the

reference supply and the pull-up resistors and output drivers, and wherein the other power supply conductor is coupled between the power supply and the primary and secondary SDRAMS".

Response to Arguments

10. Applicant's arguments with respect to amended claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Prior art

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Katsumata	Patent No.: US 5,563,773	Date of Patent: Oct. 8, 1996
Iwane	Patent No.: 5,719750	Date of Patent: Feb. 17, 1998

Contact Information

12. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (571) 272-1955. Normal contact times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703)

305-3900. The faxed phone number for organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC@uspto.gov.

Dang Nguyen 6/2/2005

6/13/05

RICHARD ELMS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800